WHAT IS CLAIMED IS:

1. A method for performing passive voltage contrast on a silicon on insulator (SOI) device comprising the steps of:

grinding a first portion of a substrate of said SOI device with a dimpling tool;

etching a second portion of said substrate of said SOI device with tetramethylammonium hydroxide (TMAH) following said grinding of said SOI device with said dimpling tool; and

directing a beam of electrons at a backside surface of said SOI device.

2. The method of claim 1, wherein said beam of electrons is operable for generating a secondary emission of electrons one or more active regions in said SOI device.

3. The method of claim 2, wherein a presence of said secondary electron emission signals determines a p-type active region, and an absence of secondary emission determines a n-type active region.

4. The method of claim 2, said secondary emission for inspecting a boundary between a first active region and a second active region of said one or more active regions in said SOI device.

5. The method of claim 1 further comprising connecting one or more pins of a pin-grid-array package containing said SOI device to a ground reference.

6. The method of claim 1 further comprising:

applying a conductive coating to a topside surface of said SOI device; and

connecting said conductive coating to a ground reference.

7. The method as recited in claim 1, wherein said conductive coating comprises a carbon ink coating.

8. The method of claim 1 further comprising etching a third portion of said substrate and a portion of a box insulator of said SOI device with hydrofluoric acid (HF) following said etching of said SOI device with said TMAH.

9. A silicon on insulator (SOI) device, comprising:

a substrate;

a box insulator overlaying said substrate wherein said box insulator has a backside surface, said backside surface having a portion exposed through said substrate; and

a body overlaying said box insulator.

10. The SOI device as recited in claim 9, further comprising a pin-grid-array package, said SOI device contained in said pin-grid-array package.

11. The SOI device of claim 9 wherein said portion exposed through said substrate is defined by grinding a portion of said substrate using a dimpling tool and subsequent etching using tetramethylammonium hydroxide (TMAH).

12. The SOI device of claim 9 wherein a portion of said box insulator is removed.

13. The SOI device of claim 9 further comprising one or more active regions disposed within said body.

14. The SOI device of claim 13 further comprising:

one or more contacts to corresponding ones of said one or more active regions; and

a conductive layer disposed on a topside surface of said SOI device, the conductive layer for interconnecting said one or more contacts to a reference potential.